PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

HIKITA et al. Art Unit: 2815

Application No.: 09/496,183 Examiner: L. CRUZ

Filed: February 2, 2000 Attorney Dkt. No.: 103213-09038

For: SEMICONDUCTOR DEVICE AND SEMICONDUCTOR CHIP FOR USE THEREIN

RESPONSE UNDER 37 CFR § 1.121

Commissioner for Patents
Washington, D.C. 20231 Date: March 19, 2001

Sir:

In response to the Office Action dated December 19, 2000, please amend the above-identified application as set forth below.

IN THE CLAIMS:

Please add the following new claims.

--8. (New) A method of manufacturing a semiconductor device, comprising:

a first step of forming, on a surface of a first semiconductor chip, a plurality of chip connection portions in standardized positions so as to fit any of a plurality of types of semiconductor chips;

a second step of forming, on a surface of a second semiconductor chip, chip connection portions, as many as or less than the chip connection portions formed on the

first semiconductor chip, in standardized positions so as to fit any of the chip connection portions formed on the first semiconductor chip; and

a third step of superposing and bonding the second semiconductor chip on the first semiconductor chip.

9. (New) A method of manufacturing a semiconductor chip comprising a step of forming a plurality of chip connection portions on a surface of the semiconductor chip,

wherein the plurality of chip connection portions are formed in positions standardized among a plurality of predetermined types of semiconductor chips.

10. (New) A semiconductor chip having, on a surface thereof, a chip connection region that fits any of a plurality of predetermined types of semiconductor chips,

wherein, in the chip connection region, chip connection portions are formed in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips, and the chip connection portions are arranged along an edge of the chip connection region.

11. (New) The semiconductor chip as claimed in claim 10,

wherein the chip connection portions are arranged also in an inner portion of the chip connection region somewhat away from the edge thereof.

12. (New) The semiconductor chip as claimed in claim 10,

wherein the chip connection region is rectangular in shape, and the chip connection portions are arranged along opposite sides of the chip connection region.

13. (New) The semiconductor chip having a plurality of chip connection portions formed on a surface thereof,

wherein the plurality of chip connection portions are arranged in positions standardized among a plurality of predetermined types of semiconductor chips, and are arranged along an edge of the semiconductor chip.

14. (New) The semiconductor chip as claimed in claim 13,

wherein the chip connection portions are arranged also in an inner portion of the semiconductor chip somewhat away from the edge thereof.

15. (New) The semiconductor chip as claimed in claim 13,

wherein the semiconductor chip is rectangular in shape, and the chip connection portions are arranged along opposite sides of the semiconductor chip.--

REMARKS

The Office Action dated December 19, 2000, has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto.

Claims 8-15 have been added to more clearly recite the elements of Applicants' invention. Applicants respectfully submit that the new claims are fully supported in the specifications and drawings, as originally filed. No new matter has been added by the above amendments, and therefore, claims 1-15 are respectfully submitted for consideration.

As a preliminary matter, the drawings were objected to as failing to comply with 37 C.F.R. § 1.84(p)(5) because they include reference numbers 171, 172, 181, 191 and

192 that are allegedly not described in the specification. Applicants respectfully disagree with the Office Action's position and refer to page 8, lines 9-14 of the specification. The above-referenced section of the specification clearly mentions and describe the reference numbers 171, 172, 181, 182, 191 and 192 illustrated in Figure 2. Accordingly, Applicants respectfully request that the objection to the drawings be withdrawn.

Claims 1-7 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wenzel et al. (U.S. Patent No. 6,150,724, hereinafter "Wenzel"). Applicants respectfully traverse this rejection and submit that each of claims 1-7, and new claims 8-15, recite subject matter that is neither disclosed nor suggested in the cited prior art.

Claim 1, upon which claim 2 is dependent, recites a semiconductor device comprising a first semiconductor chip and a second semiconductor chip superimposed on and bonded to a surface of the first semiconductor chip. The chip connection portions are arranged in standardized positions so as to fit a plurality of predetermined types of semiconductor chips in a region on the surface of the first semiconductor chip where the second semiconductor chip is bonded to the first semiconductor chip. Furthermore, the chip connection portions are arranged in standardized portions so as to fit the chip connection portions arranged on the first semiconductor chip on the second semiconductor chip.

Claim 3, upon which claims 4-5 are dependent, recites a semiconductor chip having on a surface thereof, a chip bonding region that fits one of a plurality of predetermined types of semiconductor chips, wherein in the chip bonding region, chip

connection portions are arranged in standardized positions so as to fit any of the plurality of predetermined types of semiconductor chips.

Claim 6, upon which claim 7 is dependent, recites a semiconductor chip having a plurality of chip connection portions formed on a surface thereof wherein the plurality of chip connection portions are arranged in positions standardized among a plurality of predetermined types of semiconductor chips.

Accordingly, the present invention provides a semiconductor device having a chip-on-chip structure that allows easy production of various types of semiconductor devices as a whole, and further provides a semiconductor chip for use in a semiconductor device. As such, the present invention provides an efficient and cost effective method and device for upgrading an existing system, such as increasing the capacity of a memory, increasing the number of conversion bits of A/Conversion device, or increasing the number of processing bits of a CPU.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the presently pending claims and, therefore, fails to provide the critical and non-obvious advantages which are provided by the present invention.

Wenzel discloses a bump-bonded multi-IC flip-chip semiconductor device 100. The device 100, as illustrated in Figure 5 of Wenzel, has a mother integrated circuit or chip 102 and a daughter integrated circuit or chip 104. The active surface of the mother chip 102, which contains active circuitry, faces the active surface circuitry of the daughter integrated circuit 104. In other words, the active surface of both ICs 102 and 104 are facing one another. The conductive bumps 108 are used to interconnect active circuitry and interconnect structures located on the mother integrated circuit 102 with

active circuitry or conductive structures located on the daughter integrated circuit 104. The interconnected structure of the chips 102 and 104 is coupled to a ceramic, organic, or other package 106 through conductive connection bumps 110. Central bumps 108 are used to connect two or more integrated circuits to each other while peripheral bumps 110 are used to connect the mother chip 102 to the semiconductor package 106 to enable electrical connection of the ICs 102 and 104 to an external environment.

Upon review and consideration of Wenzel, Applicants respectfully submit that each and every element recited in claims 1-7 of the present application is neither disclosed nor suggested by the cited prior art. In particular, Applicants respectfully submit that the semiconductor device having a chip-on-chip structure that is recited in the present claims is clearly distinct from that which is illustrated in Wenzel because Wenzel fails to disclose or suggest the limitation of chip connection portions arranged in standardized positions so as to fit any of a plurality of types of semiconductor chips. As discussed above, Wenzel merely discloses a bump-bonded multi-chip flip-chip device 100 formed by manufacturing a mother chip 102 having a first set 207 of bumps 212 and a second set 209 of bump contact with conductive bumps 108 used to interconnect activity circuitry and interconnect structures located on the mother integrated circuit 102 with active circuitry or conductive structures located on the daughter integrated circuit 104. Although Wenzel discloses conductive bumps 108, Applicants respectfully submit that Wenzel does not disclose or suggest the limitation of chip connection portions arranged in standardized positions so as to fit any of a plurality of types of semiconductor chips. Accordingly, Applicants respectfully submit that Wenzel fails to

disclose and suggest each and every element recited in independent claims 1, 3 and 6 of the present application.

As for dependent claims 2, 4-5 and 7, Applicants submit that each of these claims recites subject matter which is neither disclosed nor suggested by Wenzel. In particular, each of claims 2, 4-5 and 7 depends from claims 1, 3 and 6, respectively. Therefore, they inherently incorporate each and every limitation recited within claims 1, 3 and 6, therein. Therefore, Applicants submit that each of claims 2, 4-5 and 7 also recite subject matter which is neither disclosed nor suggested by Wenzel for at least the reasons set forth above with respect to claims 1, 3 and 6.

Furthermore, Applicant respectfully submits that, as a matter of law, the rejections under 35 U.S.C. §102 are improper. According to the Manual of Patent Examining Procedure ("MPEP") §2131, a reference must teach every element of the claim in order to properly anticipate a claim. In addition, the Federal Circuit ruled that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. vs. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The Federal Circuit Court also stated in a separate decision that "[t]he identical invention must be shown in a complete detail as is contained in the... claim" for the reference to anticipate the claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989). In view of the case laws and the MPEP addressing a §102 rejection, Applicant respectfully submits that the rejection is improper as a matter of law since Wenzel does not teach, disclose or suggest each and every

element as set forth in claims 1-7. Therefore, Wenzel clearly does not anticipate claim 1-7 of the present invention.

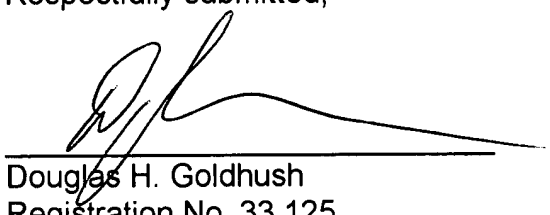
With regard to new claims 8-15, Applicants respectfully submit that each and every element recited within these claims of the present application is also neither disclosed nor suggested by Wenzel.

In view of the above, Applicants respectfully submit that claims 1-15, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully request that claims 1-15 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact by telephone the Applicants' undersigned Attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to Counsel's Deposit Account No. 01-2300.

Respectfully submitted,



Douglas H. Goldhush
Registration No. 33,125

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W.,
Suite 600
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

DHG/SH/gck